REMARKS

Rejection Under U.S.C. § 102 Rejection

The Examiner rejected claims 13 and 14 under 35 U.S.C. § 102(e) as being anticipated by Chen (U. S. Patent No. 5,885,866).

Applicant respectfully traverses this rejection and requests reconsideration of the claims for the following reasons. The Chen reference includes a bit line contact 31 and a bit line 32. Both the contact and the bit line are located vertically below the top of the cell capacitors.

Applicant notes that the present specification teaches that a region of the memory device where a contact is to be formed between memory cells can result in fabrication defects. These defects are caused by an electrical short between the bit line contact and the top electrode of a memory cell capacitor. As such, the present invention teaches that the top electrode can be excluded from the capacitor near the contact area, but cover the bottom electrode in the remaining areas. This allows for an increased lateral area to form the contact, while still providing for a large capacitive surface. For example, see Figures 11A and 11B where the contact 37 is formed between two memory cell capacitors. The contact downwardly extends from above the bottom electrode. The top electrode 24C covers the bottom electrode 20, but does not extend along the vertical surface of the bottom electrode that is adjacent the contact insulation layer 19.

Several significant differences are apparent between the claimed invention and the teachings of Chen. First, the top electrode is not common between the memory cells. Figure 12 of Chen shows a top conductor 48 that has been patterned and etched to separate the memory cells. Second, because the bit line and contact are located below the top electrode, no clearance is provided in the top electrode for the contact. Further, there is not teaching or suggestion of the contact insulation region that prevents the top electrode from extending between the bottom electrode and the contact. The pending claims, therefore, are not anticipated by the cited references.

CONCLUSION

In view of the above remarks, Applicant respectfully submits that all claims are in condition for allowance and requests reconsideration of the application and allowance of claims.

The Examiner is invited to contact Applicant's attorney to discuss any questions that may remain with respect to the present application.

Respectfully submitted,

Durcan et al.

By their Representatives,

Fogg Slifer & Polglaze, PA
P.O. Box 581009
Minneapolis, MN 55458-1009
(612) 312-2202

Date 12/21/01

By _____
Russell D. Slifer
Reg. No. 39,838

MARKED-UP VERSION OF AMENDMENTS

IN THE CLAIMS

13. (Amended) An array of capacitors, comprising:

a first bottom capacitor plate;

a second bottom capacitor plate;

a third bottom capacitor plate;

a contact between said first bottom capacitor plate and said second bottom capacitor plate, the contact downwardly extends from a vertical height above a top of the first bottom capacitor plate;

a trench between said second bottom capacitor plate and said third bottom capacitor plate;

a common top capacitor plate over said first bottom capacitor plate, said second bottom capacitor plate, and said third bottom capacitor plate, wherein said top capacitor plate extends toward said contact at a first level within said array, the top capacitor plate [and is separate from said contact] includes a lateral clearance opening at the first level around the contact, and wherein said top capacitor plate lines a side of said trench and further lines a bottom of said trench at a second level within said array; and

a dielectric between said top capacitor plate and said first, second, and third bottom capacitor plates.

67. (NEW) An array of capacitors comprising:

first, second and third memory cell capacitors comprising first, second and third bottom container-shaped electrodes, respectively;

a bit line contact laterally positioned between the first and second memory cell, the bit line contact downwardly extends from a vertical height above a top of the bottom electrode;

a trench laterally positioned between the second and third bottom electrodes to expose a portion of exterior surfaces of the second and third bottom electrodes;

a common top electrode capacitively coupled to the first, second and third electrodes via a

capacitor dielectric layer, wherein the top electrode includes a lateral clearance opening above the top of the bottom electrode and around the bit line contact; and

a bit line contact insulation region surrounding the bit line contact and filling a region between the bit line contact and the bottom electrode.

68. (NEW) An array of capacitors comprising:

first, second and third memory cell capacitors comprising first, second and third bottom container-shaped electrodes, respectively;

a bit line contact laterally positioned between the first and second memory cell, the bit line contact downwardly extends from a vertical height above a top of the bottom electrode;

a trench laterally positioned between the second and third bottom electrodes to expose a portion of exterior surfaces of the second and third bottom electrodes;

a common top electrode capacitively coupled to the first, second and third electrodes via a capacitor dielectric layer, wherein the top electrode includes a lateral clearance opening around the bit line contact; and

a bit line contact insulation region surrounding the bit line contact and filling a region between the bit line contact and the first and second bottom electrodes, wherein the bit line contact insulation region prevents the top electrode from downwardly extending between the bit line contact and the first and second bottom electrodes.